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Algorithm for Low Power IO port Design by Using CGT

Dr C. M. Jadhao

Abstract-**The Clock power is a major component of microprocessor power mainly because the clock is fed to most of the circuit blocks in the processor, and the clock switches every cycle. Thus the total clock power is a substantial component of total microprocessor power dissipation. Clock-gating is a well-known technique to reduce clock power. Because individual circuit usage varies within and across applications, not all the circuits are used all the time, giving rise to power reduction opportunity. By ANDing the clock with a gate-control signal, clock-gating essentially disables the clock to a circuit whenever the circuit is not used, avoiding power dissipation due to unnecessary charging and discharging of the unused circuits. Specifically, clock-gating targets the clock power consumed in pipeline latches and dynamic-CMOS-logic circuits (e.g., integer units, floating-point units, and word-line decoders of caches) used for speed and area advantages over static logic. Clock gating is a well-known technique to reduce chip dynamic power. This paper propose a modified clockgating techniques based on ACG(Adaptive Clock Gating) and instruction level clock gating. The proposed clock gatingtechnique reduces not only switching activity of functional blocks in IDLE state but also dynamic power in running state. Modified ACG can automatically enable or disable the clock of the functional block. The experimental results onsome I/O port core in SoC show an average of 19.45% dynamic power reduction comparing to previous ACG technique. With the scaling of technology and the need for higher performance and more functionality, power dissipation is becoming a major bottleneck for microprocessor designs. Clock power is significant in high-performance processors.**

***IndexTerms*—ACG, DCG, IO Ports, CMOS, Low Power**

I. INTRODUCTION

In recent years, the demand for power-sensitive designs has grown significantly. This tremendous demand has mainly been due to the fast growth of battery-operated portable applications such as notebook and laptop computers, personal digital assistants, cellular phones, and other portable communication devices. Semiconductor devices are aggressively scaled each technology generation to achieve high-performance and high integration density. Due to increased density of transistors in a die and higher frequencies of operation, the power consumption in a die is increasing every technology generation. Supply voltage is scaled to maintain the power consumption within limit.

The ubiquitous acceptance of portable devices such ascell phones, PDAs and mp3 players has fueled muchresearch in the development of technique for low-powerSOC.

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Dr C. M. Jadhao, Principal, Mauli College of Engineering, Shegaon-444203, India (email: cmjadhao@gmail.com)

The continuous decrease in the minimum feature size of transistors has originated a significant increase of both device density and design complexity. Recentdevice have reached such a high level of complexitywhich is implemented as a single chip. Hence, this hascome at the cost of an extremely high power demand. Alarge fraction of the overall power dissipation on a chip isdue to clock and data-path. The largest powerconsumption of a synchronous system is represented byclock distribution network, which is typically responsiblefor 30%~40% of total dynamic power dissipation [1][3].In order to limit clock power, the clock-gating approachcan be reduced power dissipation, lowering not only theswitching activity at the function unit level, but also theswitched capacitive load on the clock distributionnetwork. For these reasons, the clock -gating is regardedas one of the effective logic in RTL and architecturalpower reduction [2]. Clock gating is an effectivetechnique to reduce dynamic power [3]. Becauseindividual IP usage varies within and across applications,not all IP cores are used all the time, giving rise toopportunity for reducing the unused IP cores' power. Bycombining(AND gate) the clock with a gate-controlsignal, clock gating essentially disables the clock to an IPcore when that IP is not used, avoiding power dissipationdue to unnecessary charging and discharging of theunused circuits. In this paper, a new clock gatingtechnique for low power IP core design is introduced toavoid the limitations of traditional techniques.

II. CLOCK GATING TECHNIQUE

Several previous clock gating methods is applied indesign of micro-processor and synchronous system.Deterministic clock-gating (DCG) [1] exploits thisadvance knowledge to clock gate the unused circuits butit is fine-grained clock gating and strictly depends on thecomputer architecture. The designers have to beaccomplished in the architecture, especially the pipelines.That leads to making the design verification morecomplex. Hence, DCG is difficult to use to reduce power in the SoC design, which mainly integrates manyseparated IP cores by bus interconnections.ACG(Adaptive Clock Gating)[2] analyze the IP modelfirst. Any IP core (except combinational circuit) can bemodeled as an Finite State Machine (FSM) whichincludes several states: Idle, Ready, Run and so on, asshown in the dashed box of Fig.2. Each circle is a stateand each arrow shows a transition from a state to another.The state and the transition will be mapped to thesequential circuit and the combinational circuitrespectively by synthesis. When an IP core finishes thework, it enters the idle state and stay there until it acceptsanother request from the system bus. We call each ofthose states except Idle State

Working State. Hence, allstates in an IP core are classified to two classes: IS andWS.

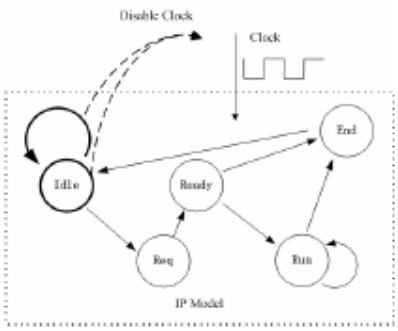

Fig 1: ACG Principle for Low Power IP Design

But ACG is only considered if any state of FSM entersthe IDLE state in Fig. 1. In case of the output controlsignals are generated in running state, these outputsignals combine with main FSM clock signal through theclock gating technique. The clock is disabledautomatically not need the clock. Therefore, ACGdisables the IP clock during the output signal is an active"high"; otherwise, the clock is enabled. It will reducemore dynamic power consumption in comparing withprevious AGC method. Hence, in this paper, we haveproposed modified AGC method in order to reduce moredynamic power consumption. To prove our proposedclock gating technology, for an example, we havepresented a sample synchronous IP called I/O portincluding in UART for low power IP design is describedin Section 3.

III. Application of Proposed Clock GatingTechnique

Dynamic power management (DPM) has been verysuccessful in low power design area. The main idea ofDPM is to reduce switching activity as much as possible;clock gating technique is used for this case. We usedinstruction level clock gating technique to control theclock of UART and I/O port. The basic procedure isshown in Fig. 2. Where PORT I/O is I/O port operation,ID is instruction decode operation, IF is instruction fetchoperation, and SIO is UART operation. Some instructions do not need SIO operation but need PORT operation,such as IN SIO, OUT SIO instruction. We can see that power control logic is used in different state of the FSMof PORT I/O functional block. The control logic makesthe decision for every instruction and every clock period,so that the clock to each component will be active modeor non-active mode corresponding to the decision. Theclock gating efficiently reduces switching of the clockand register operation in the functional blocks. Whensome of the functional blocks are in the IDLE state asmuch as possible, it reduce more the clock powerconsumption. Hence, the main idea of our proposed clockgating technique is to reduce not only the switchingactivity of a functional block in IDLE state, but also thepower consumption of a functional block in running state.The block diagram of a sample PORT I/O functionalblock is shown Fig. 3. The functional block is dividedinto three blocks: SIO (UART) block, PORT I/O block,AC(Accumulator) block. All of the operation issynchronized by the system clock, and both of the clockedge used. When a select input of SIO MUX is set to 1,PORT blocks are not used but SIO block is used. We canadopt clock gating technique to the clock of PORT block.It can disable the clock to the PORT blocks in runningstate. Hence, we can reduce power dissipation of theunused logics. Besides of measuring the powerconsumption of PORT blocks, we can also consider thepower dissipation of UART block in Fig. 3.

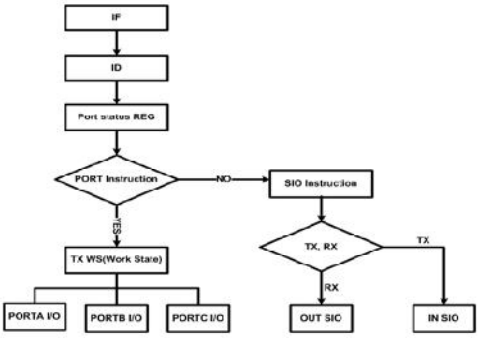

Fig 2: PORT I/O Functional Block Diagram

The sample UART is a fully functional, synthesizable,universal asynchronous receiver transmitter core in Fig. 3.The core is configurable and extremely compact. Thereceiver and the transmitter operates independently, andeach can be selectively disabled for synthesis. MostUART uses 8bits for data, no parity and 1 stop bit. Thus,it takes 10 bits to transmit a byte of data. In the UARTprotocol, the transmitter and the receiver do not share aclock signal.

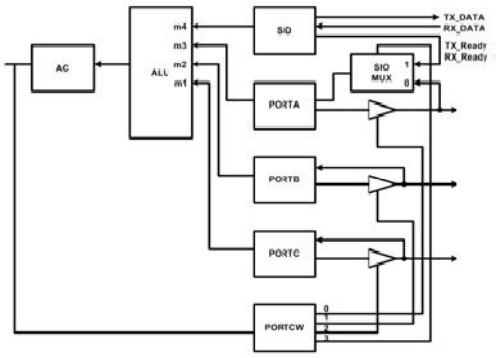

Fig 3. I/O PORT of Functional Block

Since no common clock is shared, a knowndata transfer rate (baud rate) must be agreed upon prior todata transmission. That is, the receiving UART needs toknow the transmitting UART's baud rate. In almost allcases the receiving and transmitting baud rates are thesame. The transmitter shifts out the data starting with theLSB first. The transmitter of micro-UART is composedof bit cell counter, transmitted bit counter, a serializer and a state machine which is shown as in Fig. 4

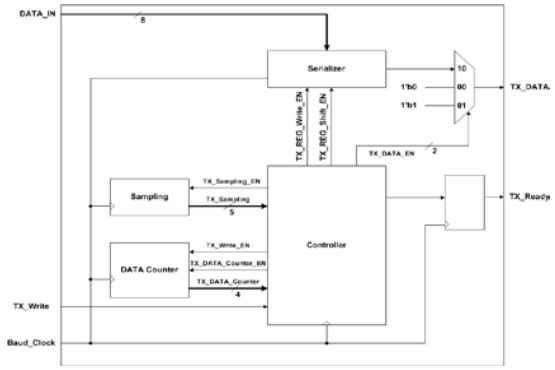

Fig 4: UART Transmitter Block

In the case of STOP state in Fig. 5, if an outputTX-total_EN signal is set to 1(high), all data bits oftransmitter are transmitted to the receiver of UART. Thisoutput signal use gated control signal bycombining (AND) the internal baud rate clock (Masterclock), is shown as Fig. 6. That is, the output signals,TX_total_EN and TX_LP_EN are active High can beresulted that there is no more clock generation anddynamic power consumption since it disables the clock oftransmitter of UART. Hence, our proposed clock gatingtechnique has no more power consumption during theperiod of an output signals is to disable the main clock oftransmitter block by using AND gate logic in IDLE statedescribed in AGC.One of the simulation results of low power transmitterof UART, In Fig. 6, CLK_gen , is disabled the clock tothe transmitter block when a signal, TX_LP_EN, is set to1 and reduce dynamic power in transmitter block.Therefore, this result verify our proposed clock gatingtechnique in IDLE state.The receiver of micro-UART is composed of a control state- machine, de-serializer, and support logic. The maingoal of the receiver is to detect the start-bit, thende-serialize the following bit-stream, detect the stop-bit,and make the data available to the host. The low powerfunctional block diagram of the receiver is shown in Fig.6. By similar above approach, the FSM of receiver ofUART, The output signal in STOP state, RX_LP_EN, isset to 1, the gated clock, CLK_gen, is disabled the clockof the receiver block. This effect also reduce the clockpower dissipation during the period of RX_LP_EN is setto 1. In other case, there is no more power consumption inreceiver block of UART, as shown in Fig. 7.

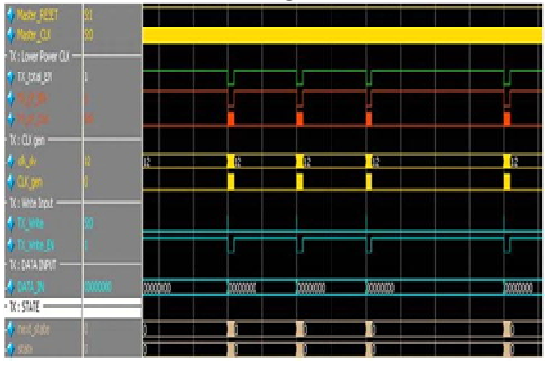

Fig. 5: Simulation Results of Transmitter block of UART

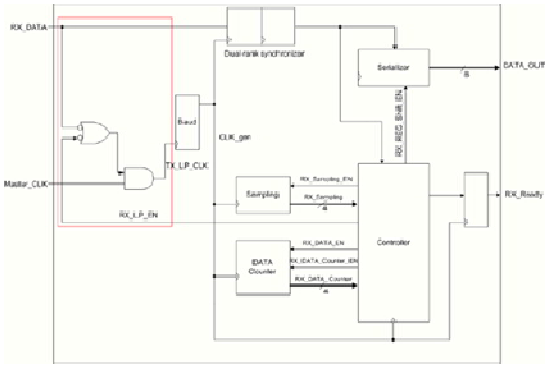

Fig 6: Low Power Receiver Functional Block of UART

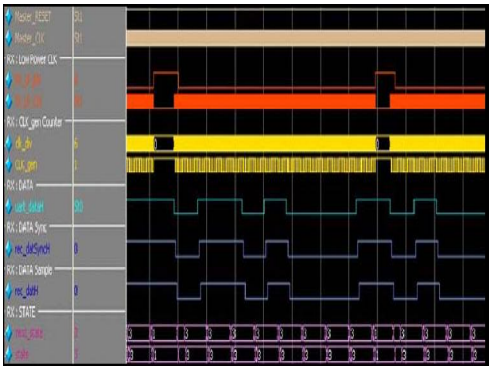

Fig. 7: Simulation Results of Receiver

Block of UART

IV Experimental Results

The experimental environment is described as below.The Synopsys power compiler and design compiler andSunOS Solaris 6.0. We use Model sim to conduct simulation and use Design Compiler of Synopsys to dosynthesis and timing analysis. Prime Power of Synopsysis also used to estimate power consumption. Typical I/OPORT benchmarks, including SIO(UART) is used toevaluate the influence on power for designs usingdifferent clock gating techniques, is shown Fig. 3. Hynix0.25-µm technology library is used to map.

We use the following flow to calculate the power of I/OPORT design. First, we synthesize the RTL source codeswith same timing constraints to two version gate level net lists, a original version and an modified ACG version.Table 1.shows that our proposed ACG reduces 16.86%dynamic power of UART, compared with the Model 1 isnot adopted clock gating technique. Table 2 also showsthat Model 2 is an application result of Prime powercompiler and our proposed ACG reduce 25.5% comparedwith the result of Prime compiler Model 1 only. Inaddition, Table 3 shows that our result reduced morepower dissipation (13.4%) than model 1 of PIC I/OPORT [3]. Hence, our modified ACG technique issignificant for low dynamic power design whensub–micron technology is used in SoC design.

Table 1: Comparison of Model 1 and Model 2 performances of UART

Power diss. of benchmrk	**Model 1**	**Model2 (ACG)**	**Experiment Result**
Cell Area	731.936 (um)	755.957(um)	+3%
Dynamic Power	100.1871(mW)	83.2954 (mW)	-16.86%

Table 2: Comparison of Model 1 and Model 2 performances of I/O PORT

Power diss. of benchmrk	**Model 1**	**Model2 (ACG)**	**Experiment Result**
Cell Area	1218.72(um)	1225.88um	+5%
Dynamic Power	164.3255(mW)	122.3254(mW)	-25.5%

Table 3: Comparison of Model 1 and Model 2 performances of PIC PORT I/O

Power diss. of benchmrk	**PIC Model 1**	**PIC Model2 (ACG)**	**Experiment Result**
Cell Area	2321.33(um)	2355.67um	+1.5%
Dynamic Power	311.244(mW)	269.45(mW)	-13.4%
Avg Dynamic Power			-19.45%

V CONCLUSION

We have proposed a modified clock gating techniques in results; we can see that the functionality and behavioral characteristics of sample UART works correctly. Using the instruction level clock gating and CG, UART and I/O PORT, we also proved that our lock gating technique is efficient for low power design in real SOC.

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