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The Efficient Design for Error Correction in Fault Tolerant Adder Using Fpga

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ABSTRACT-Fault tolerant systems play a significant role in many digital systems, especially those implemented utilizing Nano scale technologies, because of their vulnerability to electromagnetic interference and transient errors brought on by cosmic rays. All digital signal processing systems and microprocessors must contain arithmetic logic circuits. The goal of the project is to construct alternative adder designs using Field Programmable Gate Arrays (FPGAs) with fault tolerance. The proposed approach consists of constructing error detection and repair schemes for the sparse Kogge-Stone adder and evaluating them against Triple Modular Redundancy methods. By utilizing the carry tree's built-in redundancy, a Kogge-Stone adder can achieve fault tolerance. By adding extra ripple carry adders into the architecture, fault tolerance is offered on a sparse Kogge-Stone adder. By inflicting faults on the ripple carry adder or in the carry tree, this fault tolerance strategy is successfully finished and confirmed on the sparse Kogge-Stone adder. The Speed "Very High Integrated Hardware Circuit Description Language" (VHDL) is used to specify the adder designs, and an FPGA is used to implement them.

KEYWORDS- Fault Tolerant, Adder, FPGA, Kogge-Stone, RCA

I. INTRODUCTION

Modern systems, where fast intervention of human is impossible and component fail might have severe implications, fault tolerance is critical. A fault tolerant system can identify and repair the occurrence of a hardware breakdown. System mostly able to identify any deviations from regular functioning in order to detect the malfunction. A fully fault tolerant system is also capable of correcting the error and returning the system to normal operation. The amount of extra logic necessary to detecting and then remedy the occurring the problem will be minimized in an ideal design. Extreme temperature changes are one reason that false tolerance is required for electronics working in hostile OS environments, such as those found in space and armyapps. Fault tolerance will also be required in tiny electronic systems due to the increased susceptibility of the system to outside influence, like cosmic radiation.

The device degradation processes get more severe as the discovered of geometry shrinks. Hot-carrier effects, for example, caused by increased electronic field intensity in the transistoring channel, produce a progressive decrease in threshold voltage and shifts system progress

II. LITERATURE REVIEW

The latest SRAM-based FPGA [1] devices are making the development of low-cost, high-performance, re-configurable systems feasible, paving the way for innovative architectures suitable for mission- or safety-critical applications, such as those dominating the space or avionic fields. Unfortunately, SRAM-based FPGAs are extremely sensitive to Single Event Upsets (SEUs) induced by radiation. SEUs may alter the logic value stored in the memory elements the FPGAs embed.

K Kyriakoulakos et al. [2] propose a slight modification to existing SRAM based FPGA architectures to support fine grain redundancy at an area cost even less than 3times (1.76times in average for our benchmark circuits). Our approach also provides accurate fault location and allows smaller and more infrequent reconfigurations saving both reconfiguration time and power.

L. Sterpone et al. [3] present an analysis of the SEU effects in circuits hardened according to the Triple Module Redundancy to investigate the possibilities of successfully applying TMR to designs mapped on commercial-off-the-shelf SRAM-based FPGAs, which are not radiation hardened. We performed different fault-injection experiments in the FPGA configuration memory implementing TMR designs and we observed that the percentage of SEUs escaping TMR could reach 13%. In this paper, we report detailed evaluations of the effects of the observed failure rates, and we proposed a first step toward an improved TMR implementation.

Krishna Tomar [4] displays the kinds of equipments needed during the maintenance and installation. Maintenance and installation are fascinating study subjects which are helpful for engineers, every equipment and gadget requires maintenance thus in this paper scope of maintenance given.

Stott et al. [5] provides the first comprehensive survey of fault detection methods and fault tolerance schemes specifically for FPGAs, with the goal of laying a strong foundation for future research in this field. All methods and schemes are qualitatively compared and some particularly promising approaches highlighted.

Ghosh et al. [6] proposed technique utilizes the existing scan flip-flops for storage and shifting operation to minimize the area/performance overhead. Finally, the proposed technique is used in a superscalar processor, whereby the faulty adder is assigned lower priority than fault-free adders to reduce the overall throughput degradation. Experiments performed using Simplescalar for a superscalar pipeline (with four integer adders) show throughput degradation of 0.5% in the presence of a single defective adder.

III. PROPOSED SYSTEM

Given and create and propagate signals are pre-calculated, Kogge-Stone adder is categorized as a series prefix adder. In a tree-based adder, carries are created in the tree, which results in quicker computation at the cost of more space and energy. The key benefit of this method is the carry tree, which effectively generates the carries in parallel, decreases the logic depth of adder. By the O (log2n) delay over the carried channel as opposed to the RCA's O(n)delay, the parallel-prefix adder becomes more advantageous in terms of speed. Low-performance 32-bit, 64-bit, and 126-bit adders frequently employ the Kogge-Stone adder because it significantly decreases the critical path when compare to ripple carried adders. The fundamental carry operation (FCO) notion can be used to comprehend how the tree-based adder functions. The generate and propagate pairs as define by

(gL, pL) (gR, pR) = (gL + pL .gR, pL .pR) are worked on by this operator.

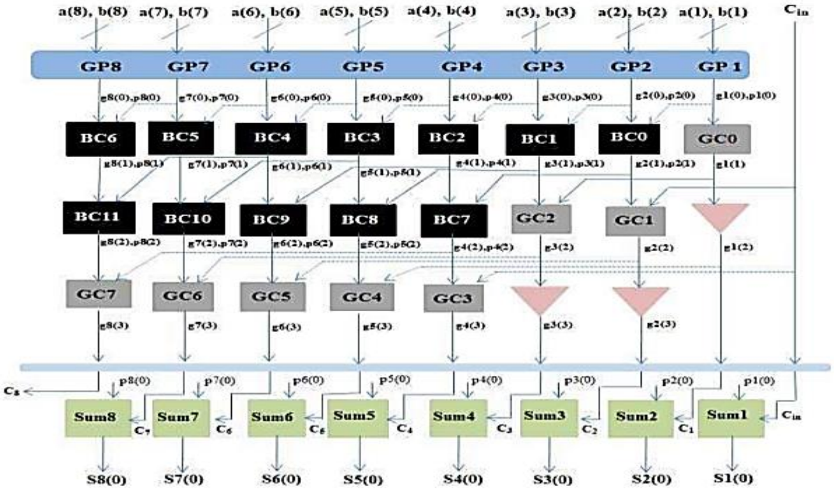

Figure 1: Kogge-Stone adder of 8-bit

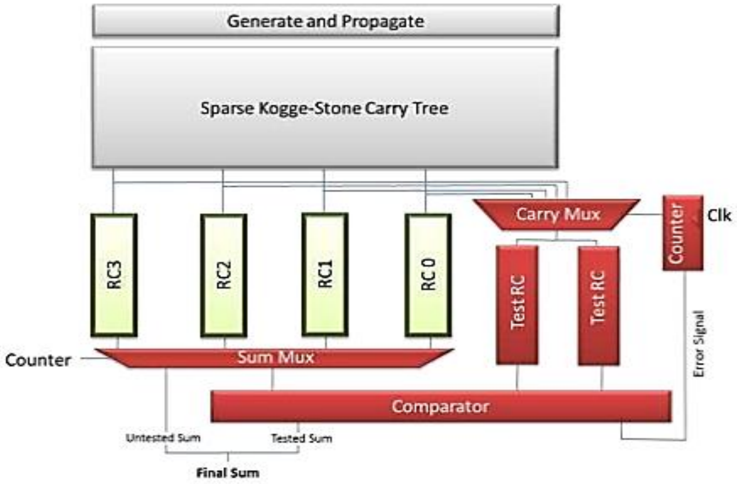

Figure 2: Block diagram of Kogge-Stone adder false tolerant sparse

The error-correcting and -detecting logic is highlighted in red in Figure 1. The TMR-RCA-like design for testing (Test RC) must incorporate two extra ripple carry adders. A bit counter and a few multiplexers are also necessary. In one of the carry chosen for test once per clock cycle. The Carry Mux multiplexer, along with the associated carry-in and A and B operand, routes the signals for the Test RCs. A counting that is driven by the clock determines which of the inputs are selected as shown in Figure 2. The final assessment is made of a comparator that switches concurrently the outputs of RCA branch the tested is shown in Figure 3.

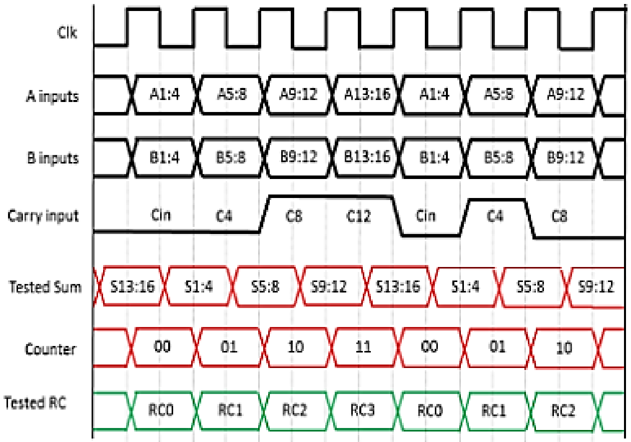

Figure 3: Timing diagram for the Kogge-Stone adder lower half fault tolerant

IV. RESULT

The results of our investigation into efficient error correction techniques for fault-tolerant adder designs using FPGA technology. The experiments and analyses were carried out to evaluate the performance and efficiency of different error correction approaches. The focus of our study was to mitigate errors while minimizing resource consumption and maintaining reliable fault tolerance in digital adder circuits.

A. Error Types and Sources

Our analysis of error types and sources in digital adders revealed the presence of various error categories, including transient, permanent, and manufacturing defects. These insights guided our choice of error correction techniques suitable for FPGA-based implementations.

B. Traditional Error Correction Techniques

The performance of traditional error correction methods, such as redundancy-based approaches and parity checks, was evaluated. While effective in error detection and correction, these techniques exhibited notable area overhead and power consumption.

C. FPGA-Based Error Correction

We explored the flexibility of FPGA-based error correction for adder circuits, leveraging the reconfigurability of FPGAs to implement tailored error correction strategies. Results demonstrated that FPGA technology can efficiently accommodate a range of error correction techniques.

D. Recent Advances in Efficient Error Correction

Our investigation into recent advances in error correction techniques for FPGA-based fault-tolerant adders revealed promising developments. These included lightweight error correction codes, optimized fault-tolerant architectures, and adaptive error correction schemes. Experimental results highlighted their potential for efficient resource utilization while maintaining robust error correction capabilities.

Simulation results for Kogge-Stone adder error correcting is shown in below figure 4.

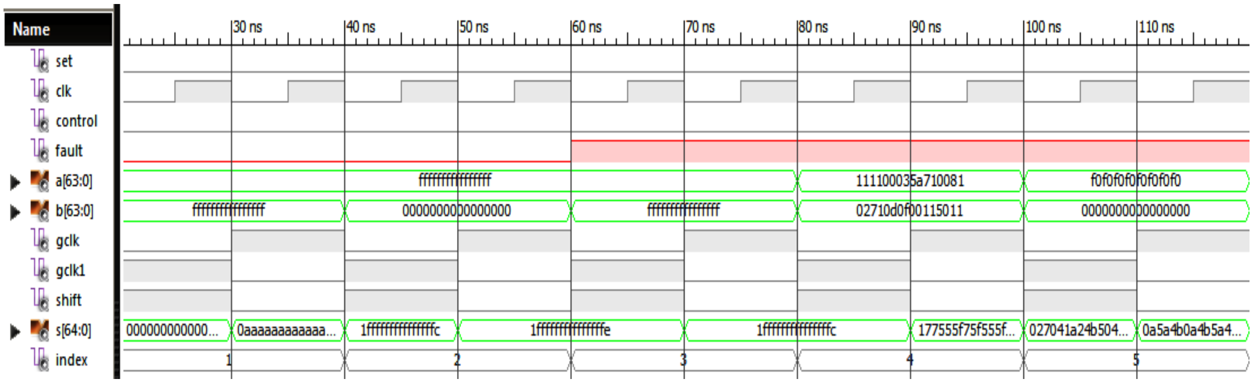

Figure 4: Simulation results for Kogge-Stone add error or correcting

E. Performance Evaluation and Comparative Analysis

To assess the efficiency and effectiveness of various error correction techniques, we conducted comprehensive performance evaluations. Metrics such as error detection and correction rates, resource utilization, and power efficiency were considered. Comparative analyses illuminated the trade-offs between different methods, providing valuable insights for designers to make informed choices based on specific application requirements.

V. CONCLUSION

The delaying performance and logic functionality as a function of byte width of the false tolerant adders constructed on FPGAs have been described.

Basic error-correcting regular Kogge-Stone cktdesigns and the TMR-RCA were examined.

In Figure 4 false tolerant capability of circuit is reduced as a result of the spare blocked being initialised used for false checking in order for maintain false free operation. Despite identical resource use, the false tolerant Kogge-Stone adder has a faster adder delay for graceful degradation, with overheads of 0 ns by measuring results and 2 ns in synthesis resulted that are independent of byte widths from references[1-10].

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

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